REMARKS

By this amendment, claim 2 is amended. Support for the amendment is found in the originally filed specification and drawings. No new matter has been added. Claims 3-9 and 11-16 are presently allowed. Claims 2-16 remain pending.

Rejection under 35 U.S.C. §102

Claim 2 was rejected under 35 USC § 102(b) as being anticipated by Kuddes (US 5,638,410). Claim 2 was also rejected under 35 USC § 102(b) as being anticipated by Hamilton (US 5,646,519).

Applicant respectfully submits that neither Kuddes nor Hamilton discloses all of the limitations recited in Applicant's amended claim 2. The amended Claim 2 recites a clock synchronization circuit comprising:

> "a programmable delay element coupled to the reference clock signal for introducing an adjustable delay in the reference clock signal to produce a delay-adjusted delayed output clock signal that becomes increasingly closer to being in synchronization with the reference clock signal; and
>
> a phase detector coupled to the reference clock signal and the delay-adjusted delayed output clock signal for detecting the phase difference between the two clock signals and for generating the in-synchronization signal when the in-synchronization state is reached."

Kuddes discloses a system for detecting and measuring a phase difference, linearly over a range of 360°, between the output signals from a primary stratum clock module (100) and a standby stratum clock module (120) in a telecommunication system. The system calculates the amount of time needed to delay a standby clock signal ($\Phi 2$) of the standby stratum clock module (120) enough to cancel the phase difference and controls a digital delay line (132) to shift the phase of the standby clock signal ($\Phi 2$) accordingly and thereby cancel the phase difference. The system includes a phase detector (124) for detecting the phase difference. The phase detector (124) generates a phase difference signal (V_{out}) as shown in Figure 3. This V_{out} signal is coupled to a low pass filter (126) which produces an output voltage according to a transfer function. The analog error voltage from the low pass filter (126) is converted to a digital signal at an A/D converter 128. The digital signal is coupled to a data input of a microprocessor 130.

It is submitted that Kuddes does not disclose, teach or suggest a number of features recited in Applicant's Claim 2. Firstly, the phase detector of Kuddes does not detect the phase difference between a reference clock signal and a delayed output clock signal that is obtained by delaying the reference clock signal as recited in Applicant's Claim 2. Instead, the phase detector of Kuddes detects the phase difference between a delayed clock signal obtained by delaying a reference clock signal ($\Phi 2$) and another reference clock signal ($\Phi 1$), which is separate from the reference clock signal ($\Phi 2$) (see Figure 1). Figure 4D of Kuddes also shows that the delayed clock signal and the reference clock signal are different signals of different duty cycles.

In addition, the phase detector of Kuddes does not produce an in-synchronization signal, especially one that includes a pulse, when the reference clock signal ($\Phi 1$) and the delayed clock signal are at least substantially in synchronization. As can be seen from Figures 4A-4C of Kuddes, the phase difference signal V_{out} from the phase detector changes in accordance to the phase difference. When two signals of the same duty cycle are in phase, V_{out} is at a logic zero or low level as shown in Figure 4A. Such a V_{out} does not include any pulse as recited in Applicant's Claim 2. When the two signals are 180° out of phase, V_{out} is at a logic one or high level as shown in Figure 4B. When the two signals are 90° out of phase, V_{out} toggles between the logic high and low levels as shown in Figure 4C. In other words, the output of the phase detector in Kuddes is a phase difference signal that is dependent on the phase difference between the two signals and not an in-synchronization signal that is generated when the in-synchronization state of the two signals is reached as recited in Applicant's Claim 2.

With regard to Hamilton, Applicant submits that it discloses a digital phase detector that includes a local oscillator 1, a programmable delay device 2, a phase lead/lag detector 3 and a delta phase modulator 9. The local oscillator 1 produces a digital clock signal C1. This clock signal C1 is inputted to the programmable delay device 2 and a clock pulse rate divider 6. The delay device delays signal C1 to produce a first delayed clock signal C2, while the divider 6 divides the frequency of clock signal C1 by two to produce a clock signal C3.

The signals C1, C2 and C3 are delivered to the lead/lag detector 3 along with a digital signal S1 having the same nominal frequency as C1 but whose phase relative to

C1 is unknown. The lead/lag detector 3 compares the phase relation between the signals S1 and C2 and outputs a signal B, which is a binary signal composed of a succession of signal segments. The phase relationship between the signals S1 and C2 is compared periodically, at the repetition frequency of signal C3, and each segment of signal has a value depending on whether C2 is leading or lagging in phase relative to S1. In one embodiment, the binary value of a segment of signal B is high, or "1", if C2 was leading S1 during the preceding sampling interval and low, or "0", if C2 was lagging S1 during the preceding sampling interval as shown in Figure 3.

The signal B is delivered to the signal input of the delta phase modulator 9. The delta phase modulator 9 produces an output signal Ph which is a multi-bit digital signal representing an estimate of the current phase of the digital signal S1 relative to the delayed clock signal C2. The output of the delta phase modulator 9 is connected to deliver the output signal Ph to a control input of the programmable delay device 2, which signal controls the magnitude of the delay to be produced by the delay device 2 in order to eliminate, or reduce, the phase difference between the signals S1 and C2. Stated in other terms, the delay device 2 is programmed by the signal Ph to produce a delay equal to, or approaching, the phase difference between S1 and C1. (See Col. 3, lines 20-60).

Applicant submits that the output signal B of the lead/lag detector 3 in Hamilton changes state only when the input signal S1 switches between leading and lagging the delayed clock signal C2, i.e. at the point where the input signal S1 and the delayed clock signal C2 are exactly synchronized or in phase. The output signal B thus does not indicate an in-synchronization state wherein the phase difference between the two clock signals is less than a predetermined value as recited in Applicant's Claim 2. Furthermore, Hamilton does not disclose an in-synchronization signal that includes a pulse as recited in Applicant's Claim 2. The output signal B in Hamilton is a step as can be seen in Figure 3.

In view of the foregoing, it is submitted that the Claim 2 is patentable over Kuddes and Hamilton individually. Withdrawal of the rejection is respectfully requested.

Rejection under 35 U.S.C. §103

Claim 10 was rejected under 35 U.S.C. 103(a) as being unpatentable over Kuddes or Hamilton.

Because Claim 10 is dependent on Claim 2, it is submitted that Claim 10 is also patentable over Kuddes and Hamilton individually for at least the same reasons stated for Claim 2. Withdrawal of this rejection is respectfully requested.

Conclusion

For the foregoing reasons, it is respectfully submitted that Claims 2-16 should be found to be in condition for allowance.

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Respectfully submitted,

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